

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	17	(optically near isolation) and (trench or opening or hole)	US-PGPUB; USPAT	OR	ON	2006/02/01 15:36
L2	182	(optically near (isolation or isolating)) and (trench or opening or hole)	US-PGPUB; USPAT	OR	ON	2006/02/01 15:37
L3	164	2 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/01 15:55
L4	2863	(trench same liner) and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/01 15:41
L5	2371	(trench with liner) and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/01 15:41
L6	1170	5 and (planarizing or planarization)	US-PGPUB; USPAT	OR	ON	2006/02/01 15:46
L7	100	6 and (optical or optically)	US-PGPUB; USPAT	OR	ON	2006/02/01 15:54
L8	2493	((optical or optically) adj (isolating or isolation))	US-PGPUB; USPAT	OR	ON	2006/02/01 15:54
L9	356	((optical or optically) adj (isolating or isolation)) with (layer or film or material)	US-PGPUB; USPAT	OR	ON	2006/02/01 16:18
L10	317	9 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/01 17:01
L11	60	((optical or optically) adj (isolating or isolation)) with (layer or film or material)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 16:57
L12	2	((optical or optically) adj (isolating or isolation)) with (silicon or polysilicon)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 16:58
L13	9	((optical or optically) adj (isolating or isolation)) same (silicon or polysilicon)	USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/02/01 17:00
L17	23864	(trench with (silicon or polysilicon))	US-PGPUB; USPAT	OR	ON	2006/02/01 17:01
L18	8158	(trench with (filled or filling) with (silicon or polysilicon))	US-PGPUB; USPAT	OR	ON	2006/02/01 17:32
L19	6880	18 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/01 17:33
L20	3481	19 and (planarizing or planarization or planarized)	US-PGPUB; USPAT	OR	ON	2006/02/01 17:33
L21	390	20 and (optical or optically)	US-PGPUB; USPAT	OR	ON	2006/02/01 17:31

L22	17051	((silicon adj carbide) or SiC or (gallium adj nitride) or GaN) with (substrate or wafer)	US-PGPUB; USPAT	OR	ON	2006/02/01 17:32
L23	2526	22 and (trench)	US-PGPUB; USPAT	OR	ON	2006/02/01 17:32
L24	695	23 and (planarizing or planarization or planarized)	US-PGPUB; USPAT	OR	ON	2006/02/01 17:33
L25	511	24 and @ad<"20031106"	US-PGPUB; USPAT	OR	ON	2006/02/01 17:33

DOCUMENT-IDENTIFIER: US 20020153529 A1

TITLE: LED array with optical isolation structure and method
of manufacturing the same

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Abstract Paragraph - ABTX (1):

A Light Emitting Diode array (LED) with an optical isolation structure and a method of manufacturing the same. The LED array with an optical isolation structure includes a substrate, a plurality of LED units and a plurality of trenches. The plural LED units and trenches are disposed on the surface of the substrate. Each trench is disposed between every two LED units and deposited with at least one reflective metal layer. The substrate of the LED array with an **optical isolation** structure is formed of a low-energy-gap semiconductor **material**, while the LED units are formed by another kind of semiconductor **material** whose energy gap is higher than the substrate. The light emitted from each LED unit is reflected by the plural trenches deposited with at least one reflective metal layer, and absorbed by the substrate with low-energy gap.

Detail Description Paragraph - DETX (14):

[0032] According to descriptions mentioned above, the first insulation **layer** 204, the first reflective metal **layer** 205 and the second insulation **layer** 206 are constructed in the plural net-like the trenches 203 disposed between the plural LED units and thus constitute an **optical isolation** structure on the substrate 201. The depth of the **optical isolation** structure, in which a first reflective metal **layer** 206 is provided, is larger than the depth of the PN junction **layer** 202 of the plural LED units. Consequently, when the light emitting from each LED unit transfers toward the transverse directions of the unit, namely T-rays, the light transmits through the first insulation layer 204 next to the emitting LED unit, and irradiates on the first reflective layer 205 next to the insulation layer 204. Then, the light is reflected by the first reflective metal layer 205, and returns back into the area of the original emitting LED unit. Further, the substrate of the LED array of the present embodiment is made of the material whose energy gap is lower than the material of the PN junction layer of the plural LED units, i.e. the substrate is made of GaAs, and the PN junction layer is made of AlGaAs. Therefore, when the light emitting from each LED unit and transfers downwardly, namely B-rays, is absorbed by the substrate 201 whose low energy gap. Thus, the cross-talk phenomenon in the traditional LED arrays is avoided by the optical isolation

structure of the LED array of the present invention successfully.

Claims Text - CLTX (2):

1. A light emitting diode array with an **optical isolation** structure, comprising: a substrate made of a semiconductor **material**; a plurality of light emitting diode units formed on said substrate, therein, each light emitting diode unit having a PN junction layer made of a semiconductor material whose energy gap is higher than said substrate; a plurality of trenches formed on said substrate, each trench is located between every two adjacent said light emitting diode units and used to isolate said adjacent plural light emitting diode units, therein, the depth of said trenches is larger than the depth of said light emitting diode units; a first insulation layer formed on said substrate, said first insulation layer is formed on the surface of said plural light emitting diode units and on the surfaces inside said plural trenches; a first reflective metal layer formed on said substrate, said first reflective metal layer is formed on the surface inside said plural trenches and overlaid on the first insulation layer formed inside said plural trenches a second insulation layer formed on said substrate, said second insulation layer is formed on the surface inside said plural trenches and overlaid on the first reflective metal layer formed inside said plural trenches; a passivation layer formed on said substrate, said passivation layer is overlaid on the surface of the first insulation layer formed on said plural light emitting diode units, and on the surface of the second insulation layer formed inside said plural trenches; a plurality of contact windows formed on said plural light emitting diode units, therein, said plural contact windows are etched through the passivation layer and the first insulation layer on said plural light emitting diode units, making part of the PN junction layer of said plural light emitting diode units exposed to said contact windows; a plurality of metal bonding pads formed on said substrate, therein, said plural metal bonding pads are connected to the PN junction layers of said plural light emitting diode units through said plural contact windows; and a backside metal layer, formed on the backside of said substrate.

Claims Text - CLTX (9):

8. A method of fabricating a light emitting diode array with an **optical isolation** structure, comprising: preparing a substrate, said substrate is made of a semiconductor **material**; forming an epitaxy layer on the surface of said substrate, said epitaxy layer is made of semiconductor material whose energy gap is higher than said substrate; transforming said epitaxy layer into a PN junction layer; patterning a plurality of light emitting diode unit areas on the surface of said PN junction layer with photolithography technology; forming a plurality of trenches and a plurality of light emitting diode units

by removing the PN junction layer and part of said substrate disposed in said plural light emitting diode unit areas, therein, the depth of said plural trenches is larger than the depth of said PN junction layer; depositing a first insulation layer on the entire surface of said substrate with a PECVD technology; depositing a first reflective metal layer on the entire surface of said substrate, said first reflective metal layer is deposited on the surface of said first insulation layer; planarizing the surface of said substrate and refilling said plural trenches by coating a second insulation layer on the entire surface of said substrate, therein, said second insulation layer is deposited on the surface of said first reflective metal layer; removing part of said secondary insulation layer with etching technology, therein, only said second insulation layer formed inside said plural trenches is remained after this step; removing part of said first reflective metal layer with etching technology, therein, only said first reflective metal layer formed inside said plural trenches is remained after this step; depositing a passivation layer on the entire surface of said substrate; patterning a plurality of contact window areas on the surface of said passivation layer with photolithography technology; forming a plurality of contact windows by removing said passivation layer and said first insulation layer exposed to said plural contact window areas with etching technology; depositing a second metal layer on the entire surface of said substrate; patterning a plurality of metal bonding pad areas on the surface of said second metal layer with photolithography technology; forming a plurality of metal bonding pads by removing part of said second metal layer with etching technology, therein, only said second metal layer formed in said plural metal bonding pad areas is remained after this step; and depositing a third metal layer on the backside of said substrate as a backside metal layer.